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### **Objection to the Specification**

Paragraph 1 of the Office Action objects to the specification. The Office Action states that the detailed description does not describe FIG. 32. Applicants respectfully disagree. FIG. 32 shows an example of a 3-phase clock that may be used in the operation of the squaring circuit of FIG. 31. Applicants admit that these exact words do not appear in the description. Nonetheless, FIG. 32 is adequately described to one of ordinary skill in the art. FIG. 32 and FIG. 31 appear on one drawing sheet. FIG. 32 clearly shows an example of a 3-phase clock, and FIG. 31, which shows one embodiment of a squaring circuit, clearly calls for a 3-phase clock. Moreover, in describing the operation of the squaring circuit of FIG. 31, the description refers to “the 3-phase clock”, “the three clock phases”, “on P1”, “on P2 of the 3-phase clock”, “on phase P3 of the 3-phase clock” (see page 32, lines 6, 10, 14, 20, 31 and page 33, line 8). There are no other figures or 3-phase clock on the drawing sheet. Fig. 6 shows a 3-phase clock but that 3-phase clock is illustrated identical to the one shown in FIG. 32.

Nevertheless, in order to further prosecution, the detailed description has been amended, along with the description of the Figures, to refer specifically to FIG. 32 as showing the 3-phase clock. No new matter has been added. Reconsideration and removal of the objection to the specification is requested.

### **Claim Amendments**

Claims 1, 17, 27 and 37 have been amended to more particularly point out and distinctly claim the invention. None of these amendments are relied upon to traverse the claim rejections, however, as discussed below. Note that although claim 17 recites “connecting at least two of the capacitors to one another”, it should be understood that this does not require that the capacitors be connected to one another directly. The specification provides support for the amendments to claims 1, 17, 27, and 37 at least, for example, at one or more portions of page 12, line 3-page 14, line 33, page 15, lines 1-2, page 15, line 5-page 21, line 6, page 23, line 5-page 25, line 8, page 27, line 14- page 28, line 26, page 29, lines 17-18, page 31, line 16-page 35, line 4.

### **New Claims**

Claims 40-64 have been added. The specification provides support for claims 40, 42, 44, 46, 48, 50, 52 and 54 at least, for example, at one or more portions of page 11, line 28 through page 12, line 2. The specification provides support for claims 41, 43, 45, 47, 49, 51, 53 and 55 at least, for example, at one or more portions of page 12, line 8 through page 20, line 30.

The specification provides support for claims 58 and 62-64 at least, for example, at original claims 1, 17, 27 and 37, respectively, and at one or more portions of page 12, line 3-page 14, line 33, page 15, lines 1-2, page 15, line 5-page 21, line 6, page 23, line 5-page 25, line 8, page 27, line 14- page 28, line 26, page 29, lines 17-18, page 31, line 16-page 35, line 4.

New claims 56-57 and 59-60 are also supported at least, for example, at one or more portions of page 12, line 3-page 14, line 33, page 15, lines 1-2, page 15, line 5-page 21, line 6, page 23, line 5-page 25, line 8, page 27, line 14- page 28, line 26, page 29, lines 17-18, page 31, line 16-page 35, line 4.

### **Claim Rejections Under 35 U.S.C. 102**

In paragraph 3 of the Office Action, claims 1-39 are rejected under 35 U.S.C. 102(b) as anticipated by Powell et al.

The Office Action states that Fig. 2 of Powell et al. discloses:

a multi bit switched capacitor DAC comprising:

a decoder 40 that receives a 4-bit binary input BO-B4 and provides multi bit digital output signals PO-P7 and N1-N8;

a switched capacitor network that includes a plurality of subDACs each of which receives an associated bit of the multi bit digital signals P0-P7 and N1-N8, and sharing capacitors 106-128;

and

an analog output signal.

Applicants traverse the rejections. As an initial matter, Applicants point out that the statement in the Office Action is merely a bold citation to a reference and does not adequately support the rejection. Applicants should not have to guess at an Examiner's reasoning. An Office Action is incomplete without a detailed application of the prior art to the claim being rejected. Applicants remind the Examiner of MPEP 706 which states that "the goal of examination is to clearly articulate any rejection early in the prosecution process so that the Applicants has the opportunity to provide evidence of patentability and otherwise reply completely at the earliest opportunity."

Nonetheless, in order to further prosecution, Applicants have made a good faith effort to try to understand and respond to all of the rejections.

If, however, the Examiner has an understanding of the reference that differs from Applicants' and he continues to believe that the claims are unpatentable over Powell et al., the Examiner is requested to issue a new, non-final Office Action that completely addresses each and every feature of the claims including a complete factual basis for any rejection.

Moreover, because the reasons set forth herein are sufficient to traverse the rejections, Applicants do not address other possible reasons why the rejection are improper.

### Claims 1-8

Claim 1 recites a DAC comprising a switched capacitor network that receives a multi-bit digital signal. The switched capacitor network has a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the DAC having a charge sharing operating state in which at least two of the plurality of sub DACs share charge with one another, and having an operating state, initiated subsequent to the charge sharing operating state, in which the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

The charge sharing required by claim 1 (both before and after amendment) is absent in Powell.

Fig. 2 of Powell et al. shows a schematic diagram for a 4-bit (16 level) embodiment of a switched capacitor DAC (col. 3, lines 35-37). The DAC includes a decoder that receives a 4-bit binary input B0-B3 and selectively drives one of sixteen output signal lines P0-P7, N1-N8 to a high state in dependence on the binary input B0-B3 (col. 3, lines 42-49). The sixteen signals are connected respectively to switches 76-104 (col. 3, lines 49-50). One terminal of each pair of switches is respectively connected to one side of capacitors 106-128 (col. 3, lines 56-57). Each of the switches 76-104 will, when closed, connect its respective capacitor (106-128) to a positive reference voltage  $+V_r$  or a negative reference voltage  $-V_r$  (col. 3, lines 64-66).

During a first clock phase,  $\phi_1$ , all eight capacitors (106-128) are simultaneously connected to ground and discharged by the closing of switches 130-134 in addition to the closing of switches 18' and 26' (col. 4, lines 10-14). During a second clock phase,  $\phi_2$ , only one of the capacitors is driven to either the positive or negative reference, as selected by the output signal

on one of the lines 44-74 (P0-P7, N1-N8) selecting the appropriate switch among switches 76-104 (col. 4, lines 15-19). All other capacitors have one plate floating so that they do not contribute sampled thermal noise or charge injection to the DAC output voltage (col. 4, lines 40-43). This causes the output voltage to be driven to a value of  $\pm(C_2/\alpha C_1) \times V_{ref}$ , where  $\alpha$  = the fraction preceding  $C_1$  of the selected capacitor shown in Fig. 2 (col. 4, lines 19-22).

Thus, Powell et al. discloses that the DAC has two different states: one state (corresponding to the first clock phase  $\phi_1$ ) in which all of the capacitors are connected to **ground/discharged**, and another state (corresponding to the second clock phase  $\phi_2$ ) in which **only one capacitor is connected** to form the DAC output voltage; all other capacitors have one plate floating so that they do not contribute sampled thermal noise or charge injection to the DAC output voltage (col. 4, lines 35-40) (emphasis added).

Consequently, in contrast to the assertion in the Office Action (which states that the capacitors 106-128 are sharing **capacitors**), **none of the capacitors 106-128 share charge** with one another in either of these two states. Capacitors do not share charge with one another when they are all connected to ground and discharged in the manner shown in FIG. 2 of Powell et al. Neither do they share charge with one another when all but one has a plate floating in the manner shown in FIG. 2 of Powell et al. In fact, Powell et al. actually teaches away from sharing charge by stating that only one capacitor is connected to form the DAC output voltage and all other capacitors have one plate floating so that they do not contribute sampled thermal noise or charge injection to the DAC output voltage (col. 4, lines 40-43).

Consequently, even if Powell et al. shows a switched capacitor network that includes a plurality of sub DACs, each of which receives an associated bit of the multi-bit digital signals P0-P7, N1-N8, as asserted in the Office Action, Powell et al. does not teach or suggest that **at least two of the plurality of sub DACs share charge with one another**, as recited in claim 1 (emphasis added).

Therefore, Powell et al. do not teach or suggest a system meeting the limitation “**at least two of the plurality of sub DACs sharing charge with one another**”, as recited in claim 1 (emphasis added).

Accordingly, claim 1 should now be allowed.

Claims 2-8, 40-41 and 56-57 depend from claim 1 and are patentable for at least the same reasons as stated above for claim 1. Reconsideration and allowance of claims 2-8, 40-41 and 56-57 is respectfully requested.

Claims 9-11

Claim 9 recites a DAC that comprises a switched capacitor network that receives an equally-weighted multi-bit digital signal and outputs one or more analog signals, wherein at least one of the one or more analog signals comprises a single packet of charge indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

The equally-weighted multi-bit digital signal and the single packet of charge indicative of a sum of equally-weighted values of each bit in the multi-bit signal recited in claim 9 are absent in Powell et al..

As stated above in regard to claim 1, Powell et al. teaches that 4-bit binary input B0-B3 represents 16 levels (col. 3, line 35) and that the decoder selectively drives 1 of the 16 output signal lines 44-74, i.e., P0-P7, N1-N8, in dependence upon the 4-bit binary input (col. 3, lines 46-49).

Thus, the 4-bit binary input B0-B3 and the decoded output signals P0-P7, N1-N8 are each binary weighted signals. Indeed, it would appear that neither the 4-bit binary input B0-B3 nor the decoded output signals P0-P7, N1-N8 can be considered an equally-weighted multi-bit digital signal. Neither the 4-bit binary input B0-B3 nor the decoded output signals P0-P7, N1-N8 appear to have any bits that are equally-weighted.

Consequently, Fig. 2 of Powell et al. does not teach or suggest a switched capacitor network that receives an **equally-weighted multi-bit digital signal** and outputs one or more analog signals, wherein at least one of the one or more analog signals comprises a single packet of charge indicative of a **sum of equally-weighted values** of each bit in the multi-bit signal, as recited in claim 9 (emphasis added).

Therefore, Powell et al. does not teach or suggest a DAC that comprises a switched capacitor network “that receives an **equally-weighted multi-bit digital signal** and outputs one or more analog signals, wherein at least one of the one or more analog signals comprises a single packet of charge indicative of a **sum of equally-weighted values** of each bit in the multi-bit signal”, as recited in claim 9 (emphasis added).

Accordingly, claim 9 should be allowed.

Claims 10-11 depend from claim 9 and are patentable for at least the same reasons as stated above for claim 9. Reconsideration and allowance of claims 10-11 is respectfully requested.

Claims 12-16, 65

Claim 12 recites a DAC that comprises a switched capacitor network that receives an equally-weighted multi-bit digital signal, the switched capacitor network having a plurality of sub DACs, at least two of the plurality of sub DACs sharing charge with one another, wherein the switched capacitor network outputs an analog signal indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

Powell et al. does not teach or suggest an **equally-weighted multi-bit digital signal**. Neither does Powell et al. teach or suggest **at least two of the plurality of sub DACs sharing charge with one another**, as recited in claim 12 (emphasis added).

Therefore, Powell et al. does not teach or suggest a DAC comprising a switched capacitor network “that receives an **equally-weighted multi-bit digital signal**, the switched capacitor network having a plurality of sub DACs, **at least two of the plurality of sub DACs sharing charge with one another**, wherein the switched capacitor network outputs an analog signal indicative of a **sum of equally-weighted values of each bit in the multi-bit signal**”, as recited in claim 12 (emphasis added).

Accordingly, claim 12 should now be allowed.

Claims 13-16, 42-43 and 65 depend from claim 12 and are patentable for at least the same reasons as stated above for claim 12. Reconsideration and allowance of claims 13-16, 42-43 and 65 is hereby respectfully requested.

Claims 17-20

Claim 17 recites a method of converting a multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal. The method comprises charging each of a plurality of capacitors to a value corresponding to a value of a bit in the multi-bit signal, wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit, temporarily connecting at least two of the plurality of capacitors to one another to share charge, and providing at least one analog output signal indicative of a sum of values of each bit in the multi-bit signal, after disconnecting the at least two of the plurality of capacitors from one another.

As explained above, Powell et al. does not teach or suggest charging a plurality of capacitors to a value corresponding to a value of a bit in the multi-bit signal and connecting at

least two of the plurality of capacitors to one another to **share charge**, which is recited in claim 17 (emphasis added). Consequently, Powell et al. does not anticipate claim 17.

Accordingly, claim 17 should now be allowed.

Claims 18-20 and 44-45 depend from claim 17 and are patentable for at least the same reasons as stated above for claim 17. Reconsideration and allowance of claims 18-20 and 44-45 is hereby respectfully requested.

#### Claims 21-23

Claim 21 recites a method of converting an equally-weighted multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal. The method comprises charging each of a plurality of capacitors to a value corresponding to a value of a bit in the equally-weighted multi-bit signal, and generating a single packet of charge on at least one capacitor indicative of a sum of equally weighted values of each bit in the multi-bit signal.

As stated above for claim 9, Powell et al. does not teach or suggest an **equally-weighted multi-bit digital signal** or a single packet of charge indicative of a **sum of equally-weighted values** of each bit in the multi-bit signal (emphasis added). Consequently, Powell et al. does not anticipate claim 21.

Accordingly, claim 21 is allowable.

Claims 22-23 depend from claim 21 and are patentable for at least the same reasons as stated above for claim 21. Reconsideration and allowance of claims 22-23 is hereby respectfully requested.

#### Claims 24-26

Claim 24 recites a method of converting an equally-weighted multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal. The method comprises charging each of a plurality of capacitors to a value corresponding to a value of a bit in the equally-weighted multi-bit signal, and connecting at least two of the plurality of capacitors to one another to share charge.

As stated above for claim 12, Powell et al. does not teach or suggest an **equally-weighted multi-bit digital signal**. Nor does Powell et al. teach or suggest charging a plurality of capacitors to a value corresponding to a value of a bit and connecting at least two of the plurality

of capacitors to one another to **share charge**. Consequently, Powell et al. does not anticipate claim 24.

Accordingly, claim 24 is allowable.

Claims 25-26 and 46-47 depend from claim 24 and are patentable for at least the same reasons as stated above for claim 24. Reconsideration and allowance of claims 25-26 and 46-47 is hereby respectfully requested.

#### Claims 27-30

Claim 27 recites a DAC that comprises means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in a multi-bit signal, wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit, means for temporarily connecting at least two of the plurality of capacitors to one another to share charge, and means for providing at least one analog output signal indicative of a sum of values of each bit in the multi-bit signal, after disconnecting the at least two of the plurality of capacitors from one another.

As stated above for claim 17, Powell et al. does not teach or suggest charging a plurality of capacitors to a value corresponding to a value of a bit and connecting at least two of the plurality of capacitors to one another to **share charge**. Consequently, Powell et al. does not anticipate claim 27.

Accordingly, claim 27 is allowable.

Claims 28-30 and 48-49 depend from claim 27 and are patentable for at least the same reasons as stated above for claim 27. Reconsideration and allowance of claims 28-30 and 48-49 is hereby respectfully requested.

#### Claims 31-33

Claim 31 recites a DAC that comprises means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in an equally-weighted multi-bit signal, and means for generating a single packet of charge on at least one capacitor indicative of a sum of equally-weighted values of each bit in the multi-bit signal .

As stated above for claim 21, Powell et al. does not teach or suggest an **equally-weighted multi-bit digital signal** or a single packet of charge indicative of a **sum of equally-weighted**

**values** of each bit in the multi-bit signal. Consequently, Powell et al. does not anticipate claim 31.

Accordingly, claim 31 is allowable.

Claims 32-33 depend from claim 31 and are patentable for at least the same reasons as stated above for claim 31. Reconsideration and allowance of claims 32-33 is hereby respectfully requested.

#### Claims 34-36

Claim 34 recites a DAC that comprises means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in an **equally-weighted** multi-bit signal, and means for connecting at least two of the plurality of capacitors to one another to share charge.

As stated above for claim 24, Powell et al. does not teach or suggest an **equally-weighted multi-bit digital signal**. Nor does Powell et al. teach or suggest charging a plurality of capacitors to a value corresponding to a value of a bit and connecting at least two of the plurality of capacitors to one another to **share charge**. Consequently, Powell et al. does not anticipate claim 34.

Accordingly, claim 34 is allowable.

Claims 35-36 and 50-51 depend from claim 34 and are patentable for at least the same reasons as stated above for claim 34. Reconsideration and allowance of claims 35-36 and 50-51 is hereby respectfully requested.

#### Claim 37

Claim 37 recites an integrated circuit that comprises an integrated a switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the DAC having a charge sharing operating state in which at least two of the plurality of sub DACs share charge with one another, and having an operating state, initiated subsequent to the charge sharing operating state,

in which the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

As stated above for claim 1, Powell et al. does not teach or suggest that **at least two of the plurality of sub DACs share charge with one another**. Consequently, Powell et al. does not anticipate claim 37.

Accordingly, claim 37 is allowable.

Claims 52-53 depend from claim 37 and are patentable for at least the same reasons as stated above for claim 37. Allowance of claims 52-53 is hereby respectfully requested.

#### Claim 38

Claim 38 recites an integrated circuit that comprises an integrated switched capacitor network that receives an equally-weighted multi-bit digital signal and outputs one or more analog signals, wherein at least one of the one or more analog signals comprises a single packet of charge indicative of a sum of equally weighted values of each bit in the multi-bit signal.

As stated above for claim 9, Powell et al. does not teach or suggest a switched capacitor network that receives an **equally-weighted multi-bit digital signal** and outputs one or more analog signals, wherein at least one of the one or more analog signals comprises a single packet of charge indicative of a **sum of equally-weighted values** of each bit in the multi-bit signal. Consequently, Powell et al. does not anticipate claim 38.

Accordingly, claim 38 is allowable.

#### Claim 39

Claim 39 recites an integrated circuit that comprises an integrated switched capacitor network that receives an equally-weighted multi-bit digital signal, the switched capacitor network having a plurality of sub DACs, at least two of the plurality of sub DACs sharing charge with one another, wherein the switched capacitor network outputs an analog signal indicative of a sum of equally weighted values of each bit in the multi-bit signal.

As stated above for claim 12, Powell et al. does not teach or suggest an **equally-weighted multi-bit digital signal**. Nor does Powell et al. teach or suggest **at least two of the plurality of sub DACs sharing charge with one another**. Consequently, Powell et al. does not anticipate claim 39.

Accordingly, claim 39 is allowable.

Claims 54-55 depend from claim 39 and are patentable for at least the same reasons as stated above for claim 39. Allowance of claims 54-55 is hereby respectfully requested.

**Remarks in Regard to New Independent Claims and Claims Depending Therefrom**

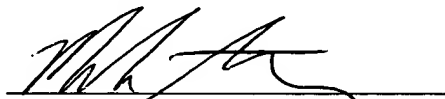
Claims 58-64 recite that at least two of the plurality of sub DACs share charge with one another, and are therefore also patentable over Powell et al..

**Conclusion**

This application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this Amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicants' Attorney at the number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby request any necessary extension of time. If there is a fee occasioned by this response, including any extension fee that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,



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**MARKED-UP SPECIFICATION**

Please amend the paragraph beginning on page 9, line 20 to read as follows:

FIG. 32 shows a three phase clock [is a block diagram of one embodiment of a squaring circuit];

Please amend the paragraph beginning on page 32, line 5 to read as follows:

FIGS. 33A-33C are block diagrams showing the operation of the squaring circuit 500 of FIG. 31 for each of the three clock phases (see FIG. 32) in the event that input terminals 512, 514, 516, 518 are supplied with digital bit signals  $bit_1$ ,  $bit_2$ ,  $bit_3$ ,  $bit_4$ , having logic states of 1, 0, 0, 0, respectively. Tables show the relationship between the clock phase, and the state (i.e., voltage and charge) of the capacitors in the one-bit DACs. Referring now to FIG. 33A, on phase P3 of the 3-phase clock (FIG. 32), all of the charge sharing switches S200, S201, S202, and S203 and the output switch S204, are in the open condition. The capacitor C1 is charged to  $V_{ref}$  in response to the logic state 1 on terminal 512. Capacitors C2, C3 and C4 are all discharged to ground in response to the logic state 0 signals on terminals 514, 516, 518, respectively. Referring now to FIG. 33B, on phase P1 of the 3-phase clock (FIG. 32) all of the charging switches S3, S6, S9 and S12 (FIG. 31) and the output switch S204 are in an open condition, and all of the charge sharing switches S200, 201, 202, 203 are in a closed condition, whereby charge is redistributed and resulting in the total charge on all of the capacitors being divided among all of the capacitors. If the capacitors C1, C2, C3, C4 all have the same capacitance value C, then the charge is shared equally so that the voltage across each capacitor becomes  $V_{ref}/4$ . Referring now to FIG. 33C, on P2 of the 3-phase clock (FIG. 32) switch S200 is in the closed condition because P2 has a logic 1 state and  $bit_1$  has a logic state 1. Switches S201, S202, S203 are in the open condition because  $bit_2$ ,  $bit_3$ ,  $bit_4$ , have a logic state 0. Output switch S204 is in the closed condition, and capacitor C1 (FIG. 31) of one-bit DAC 162 delivers its charge to the output terminal 510. Consequently, the total charge delivered to the output terminal 510 is equal to  $C \cdot V_{ref}/4$ .

Please amend the paragraph beginning on page 32, line 26 to read as follows:

FIGS. 34A-34C are block diagrams showing the operation of the squaring circuit 500 of FIG. 31 for each of the 3 clock phases in the event that input terminals 512, 514, 516, 518 are

supplied with digital bit signals  $bit_1$ ,  $bit_2$ ,  $bit_3$ ,  $bit_4$ , having logic states of 1, 1, 0, 0, respectively. Tables show the relationship between the clock phase, and the state (i.e., voltage and charge) of the capacitors in the one-bit DACs. Referring now to FIG. 33A, on phase P3 of the 3-phase clock (FIG. 32), all of the charge sharing switches S200, S201, S202, and S203 and the output switch S204, are in the open condition. The capacitor C1 and the capacitor are each charged to  $V_{ref}$  in response to the logic state 1 on terminal 512 and 514, respectively. Capacitors C3 and C4 are all discharged to ground in response to the logic 0 signals on terminals 516, 518, respectively. Referring now to FIG. 34B, on phase P1, all of the charging switches S3, S6, S9 and S12 (FIG. 31) and the output switch S204 are in an open condition, and all of the charge sharing switches S200, 201, 202, 203 are in a closed condition, whereby charge is redistributed and resulting in the total charge on all of the capacitors being divided among all of the capacitors. If the capacitors C1, C2, C3, C4 all have the same capacitance value C, then the charge is shared equally so that the voltage across each capacitor becomes  $V_{ref}/2$ . Referring now to FIG. 33C, on [1] phase P2 of the 3-phase clock (FIG. 32), switch S200 is in the closed condition because P2 has a logic state 1 and  $bit_1$  has a logic state 1. Switch S201 is in the closed condition because P2 has a logic state 1 and  $bit_2$  has a logic state 1. Switches S202, S203 are in the open condition because  $bit_3$ ,  $bit_4$ , have a logic state 0. Output switch S204 is in the closed condition, and capacitors C1 and C2 (FIG. 31) of one-bit DACs 162, 164 delivers charge to the output terminal 510. Consequently, the total charge delivered to the output terminal 510 is equal to  $C \cdot V_{ref}$ .

**MARKED-UP CLAIMS**

1. (Amended) A DAC comprising:

a switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the DAC having a charge sharing operating state in which at least two of the plurality of sub DACs share [sharing] charge with one another, and having an operating state, initiated subsequent to the charge sharing operating state, in which the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

2. (Amended) The DAC of claim 1, wherein the multi-bit digital signal is an equally-weighted multi-bit digital signal, and the associated amount of charge is the same for each of the plurality of sub DACs

3. (Amended) The DAC of claim 1, wherein the multi-bit digital signal is an equally-weighted multi-bit digital signal, and the associated capacitance is the same for each of the plurality of sub DACs.

7. (Amended) The DAC of claim 1, wherein the DAC comprises a plurality of switched capacitor cells used in forming the switched capacitor network, each of at least two of the plurality of switched capacitor cells has a orientation direction, and the at least two of the plurality of switched capacitor cells are oriented such that the orientation direction of at least one of the at least two of the plurality of switched capacitor cells is angularly offset [rotated substantially ninety degrees] relative to the orientation direction of at least one other of the at least two [one] of the plurality of switched capacitor cells, the angular offset being substantially, ninety degrees.

8. (Amended) The DAC of claim 1, wherein the DAC comprises a plurality of switched capacitor cells used in forming the switched capacitor network, each of at least four of the

plurality of switched capacitor cells has [have] a orientation direction, and the orientation direction of each one of the at least four of the plurality of switched capacitor cells [has an] is angularly offset relative to the orientation directions of the others of the at least four of the plurality of switched capacitor cells .

9. (Amended) A DAC comprising:

a switched capacitor network that receives an equally-weighted multi-bit digital signal and outputs one or more analog signals, wherein at least one of the one or more analog signals comprises a single packet of charge indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

12. (Amended) A DAC comprising:

a switched capacitor network that receives an equally-weighted multi-bit digital signal, the switched capacitor network having a plurality of sub DACs, at least two of the plurality of sub DACs sharing charge with one another, wherein the switched capacitor network outputs an analog signal indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

15. (Amended) The DAC of claim 12, wherein the DAC comprises a plurality of switched capacitor cells used in forming the switched capacitor network, each of at least two of the plurality of switched capacitor cells has a orientation direction, and the at least two of the plurality of switched capacitor cells are oriented such that the orientation direction of at least one of the at least two of the plurality of switched capacitor cells is angularly offset [rotated substantially ninety degrees] relative to the orientation direction of at least one other of the at least two [one] of the plurality of switched capacitor cells.

16. (Amended) The DAC of claim 12, wherein the DAC comprises a plurality of switched capacitor cells used in forming the switched capacitor network, each of at least four of the plurality of switched capacitor cells has [have a] an orientation direction, and the orientation direction of each one of the at least four of the plurality of switched capacitor cells [has an] is angularly offset relative to the orientation directions of the others of the at least four of the plurality of switched capacitor cells .

17. (Amended) A method of converting a multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal comprising [the steps of]:  
charging each of a plurality of capacitors to a value corresponding to a value of a bit in the multi-bit signal, wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit; [and]  
temporarily connecting at least two of the plurality of capacitors to one another to share charge [with one another]; and  
providing at least one analog output signal indicative of a sum of values of each bit in the multi-bit signal, after disconnecting the at least two of the plurality of capacitors from one another.

21. (Amended) A method of converting a equally-weighted multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal comprising [the steps of]:

charging each of a plurality of capacitors to a value corresponding to a value of a bit in the equally-weighted multi-bit signal, and  
generating a single packet of charge on at least one capacitor indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

24. (Amended) A method of converting an equally weighted multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal comprising [the steps of]:

charging each of a plurality of capacitors to a value corresponding to a value of a bit in the equally-weighted multi-bit signal , and

connecting at least two of the plurality of capacitors to one another to share charge [with one another].

27. (Amended) A DAC comprising:

means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in [the] a multi-bit signal, wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit; [and]

means for temporarily connecting at least two of the plurality of capacitors to one another to share charge [with one another]; and

means for providing at least one analog output signal indicative of a sum of values of each bit in the multi-bit signal, after disconnecting the at least two of the plurality of capacitors from one another.

31. (Amended) A DAC comprising:

means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in [the] an equally-weighted multi-bit signal, and

means for generating a single packet of charge on at least one capacitor indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

34. (Amended) A DAC comprising:

means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in [the] an equally-weighted multi-bit signal, and

means for connecting at least two of the plurality of capacitors to one another to share charge [with one another].

37. (Amended) An integrated circuit comprising:

an integrated [a] switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the DAC having a charge sharing operating state in which at least two of the plurality of sub DACs share [sharing] charge with one another, and having an operating state, initiated subsequent to the charge sharing operating state, in which the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

38. (Amended) An integrated circuit comprising:

an integrated switched capacitor network that receives an equally-weighted multi-bit digital signal and outputs one or more analog signals, wherein at least one of the one or more analog signals comprises a single packet of charge indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

39. (Amended) An integrated circuit comprising:

an integrated switched capacitor network that receives an equally-weighted multi-bit digital signal, the switched capacitor network having a plurality of sub DACs, at least two of the plurality of sub DACs sharing charge with one another, wherein the switched capacitor network outputs an analog signal indicative of a sum of equally-weighted values of each bit in the multi-bit signal.